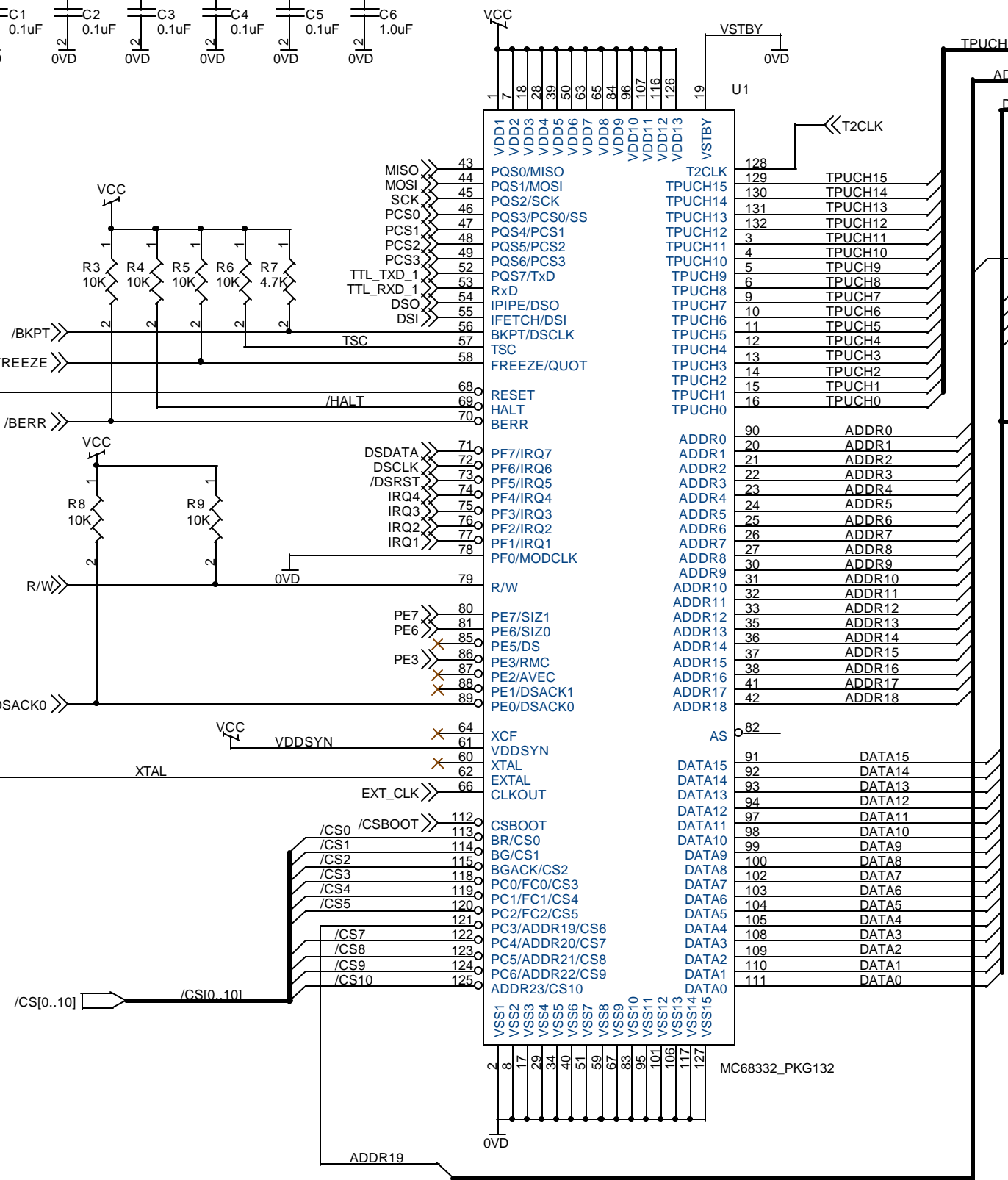
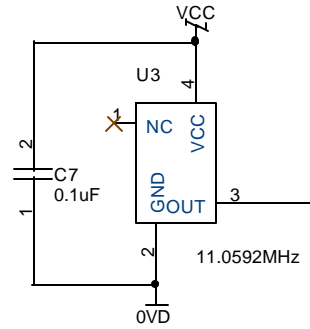
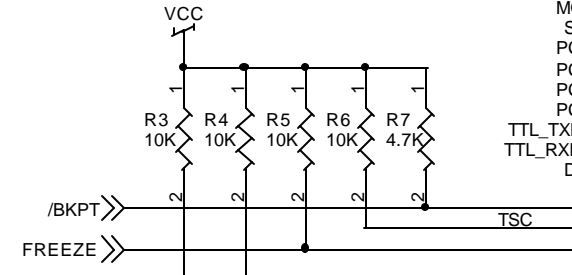
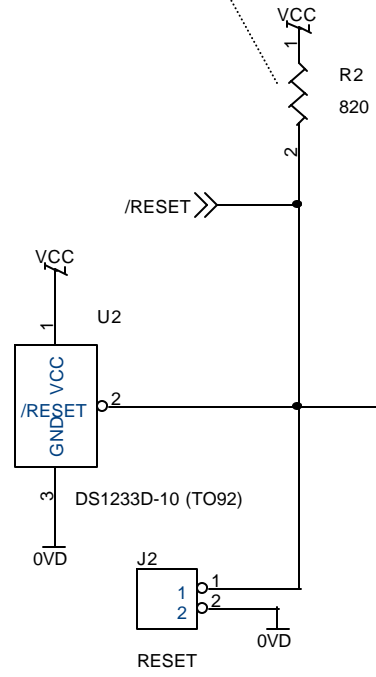
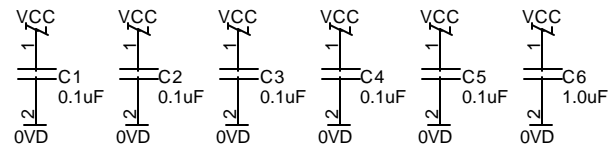


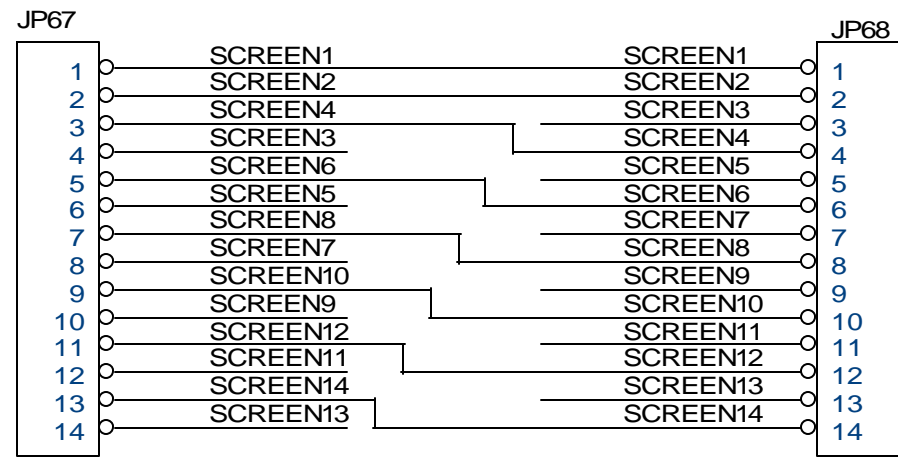
PART ONLY REQUIRED IF IMPLEMENTATION CAUSES PROBLEMS COMMING OUT OF RESET.

ALL DECOUPLING CAPACITORS IN THIS DESIGN ARE CERAMIC MONOLITICH EPOXY DIPPED.



THE LCD USES THE MODIFIED CHIP SELECT #2 (/MCS2) WHICH IS DERIVED THROUGH A STATE MACHINE IN THE CPLD. THIS IS REQUIRED FOR THE SLOW ACCESS REQUIRED BY THE DEVICE THAT IS SLOWER THAN THE OVER-RIDE SPEED OF THE PROCESSOR. THE CPLD ASSERTS ACCESS ON THE FALLING EDGE OF /CS2 WHICH DOES NOT GENERATE A DSACK. AFTER WAITING 23 CLOCK CYCLES, THE CPLD THEN GENERATES THE /DSACK0 LINE TO TERMINATE THE BUS CYCLE.

Title			CPU_&_LCD		
Size	Document Number				Rev
B	MC_332_20.DSN				P2
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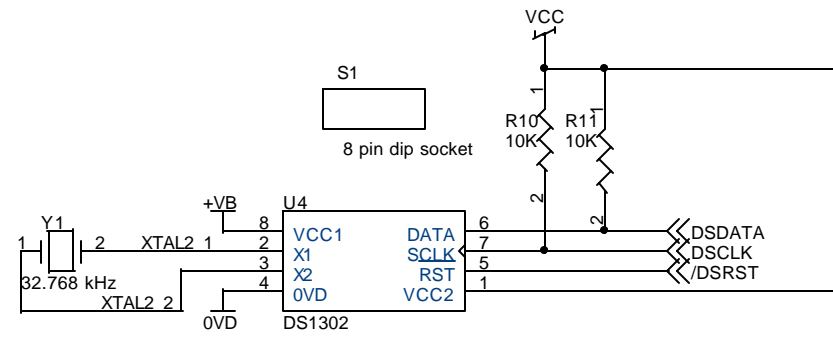
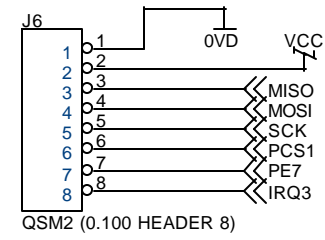
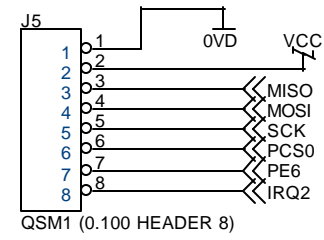
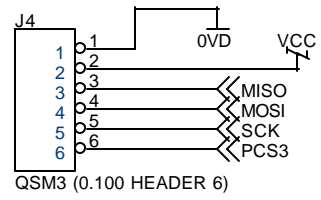
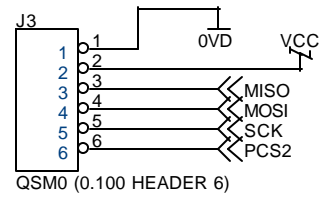


CRC332 - LCD HEADER PINS

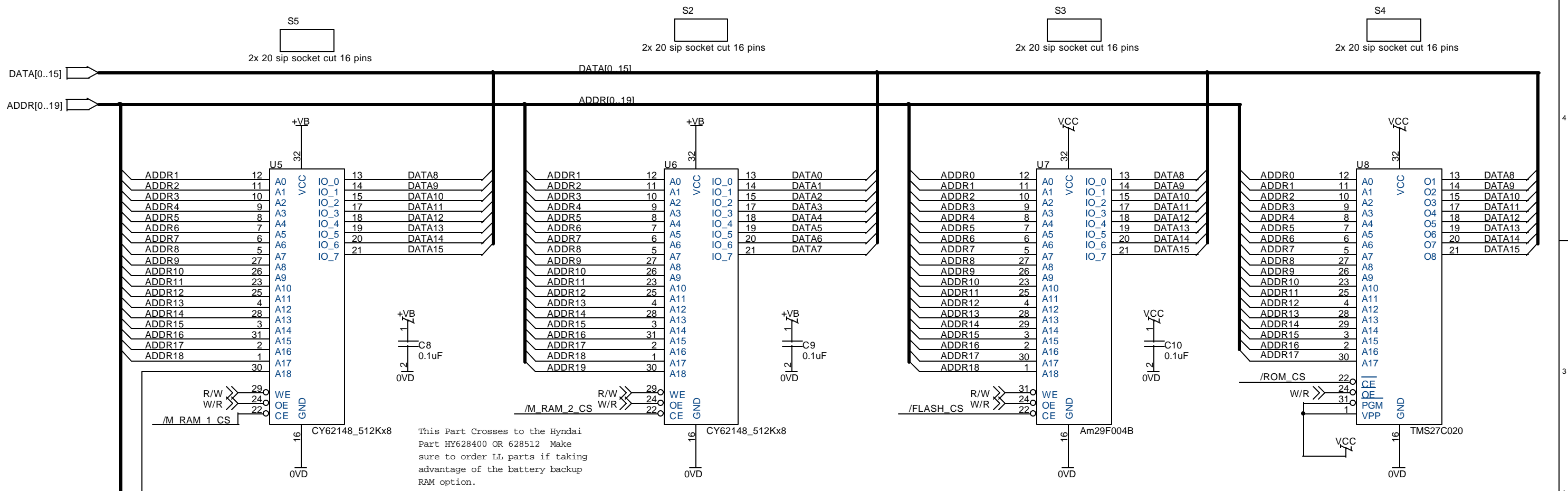
LCD SCREEN

NOTE PINS 1 & 2 ARE STRAIGHT THROUGH WHILE
3-14 ARE SWAPPED IN PAIRS

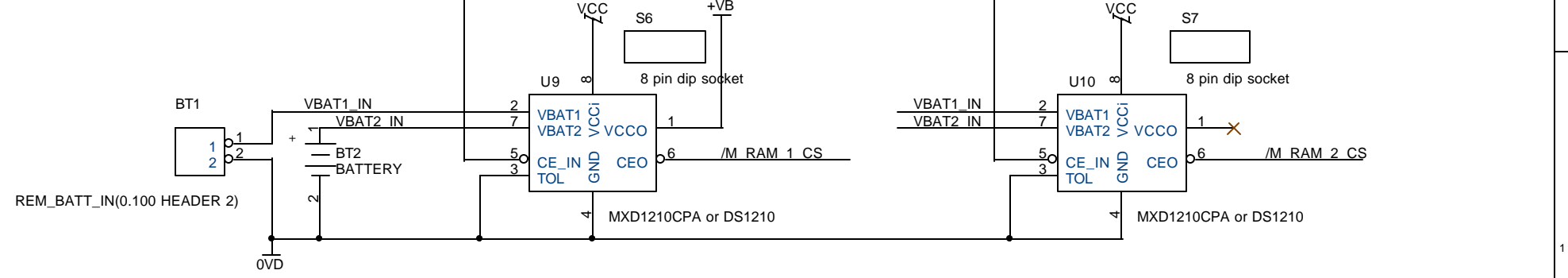
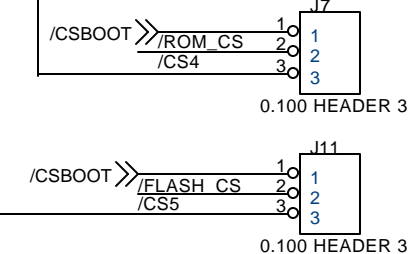
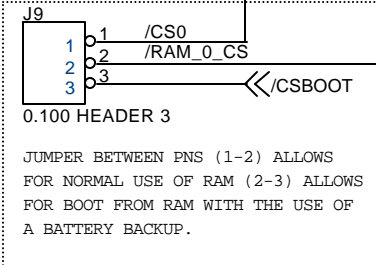
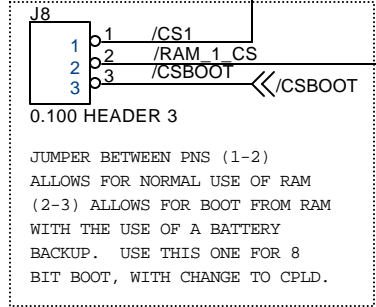
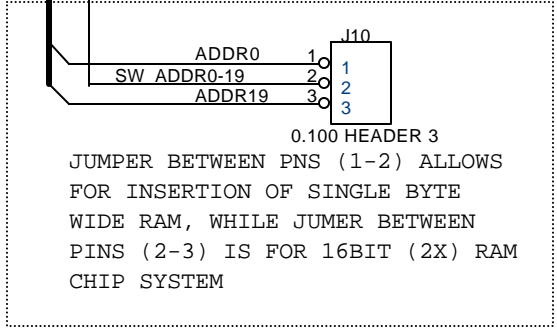
Title		
LCD_CABLE_WIRING_DIAGRAM		
Size	Document Number	Rev
A	MC332_20	P2
Date:	Tuesday, July 11, 2000	Sheet 1 of 1



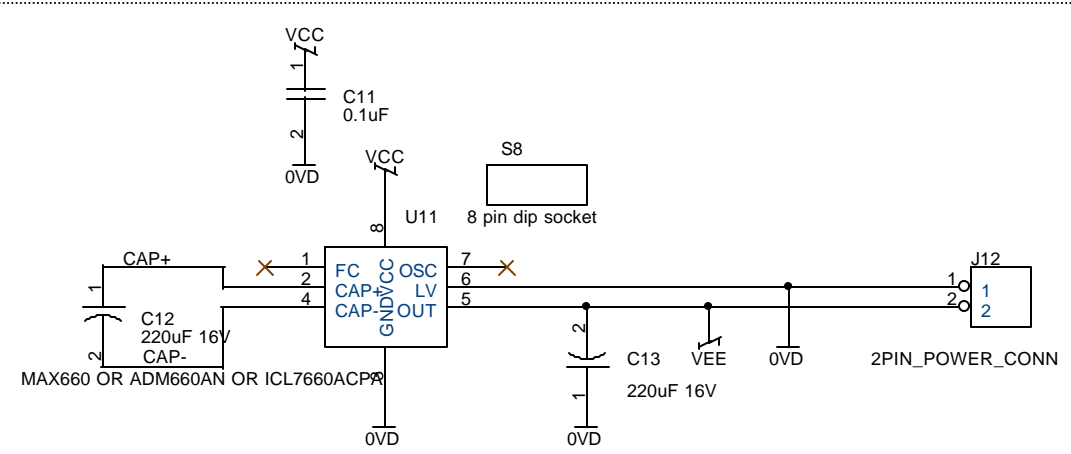
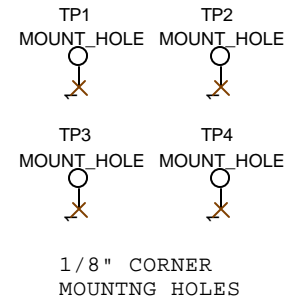
Title		
SPI_INTERFACE_CONNECTORS		
Size	Document Number	Rev
B	MC_332_20.DSN	P2
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This Part Crosses to the Hyndai Part HY628400 OR 628512 Make sure to order LL parts if taking advantage of the battery backup RAM option.

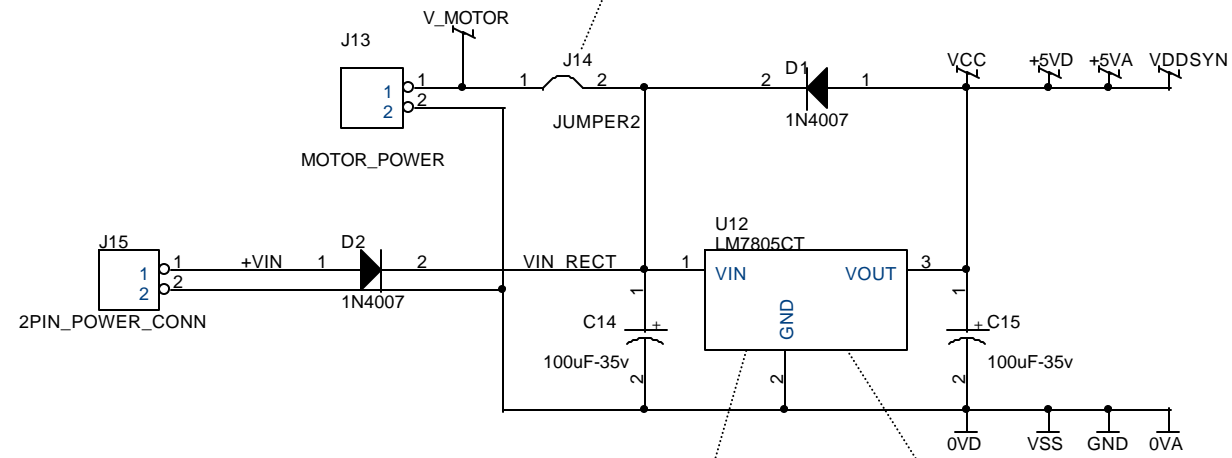


Title		
BATTERY_BACKUP & MEMORY		
Size	Document Number	Rev
B	MC_332_20.DSN	P2
Date:	Tuesday, May 30, 2000	Sheet 3 of 9



WARNING! The processor subsection has no tolerance for negative biased voltages. Unless specifically using VEE to power op-amps for the ADC or to provide contrast for the LCD, it is recommended that the MAX660 and associated capacitors not be populated to provide protection from accidental shorting to data, address or other voltage sensitive lines.

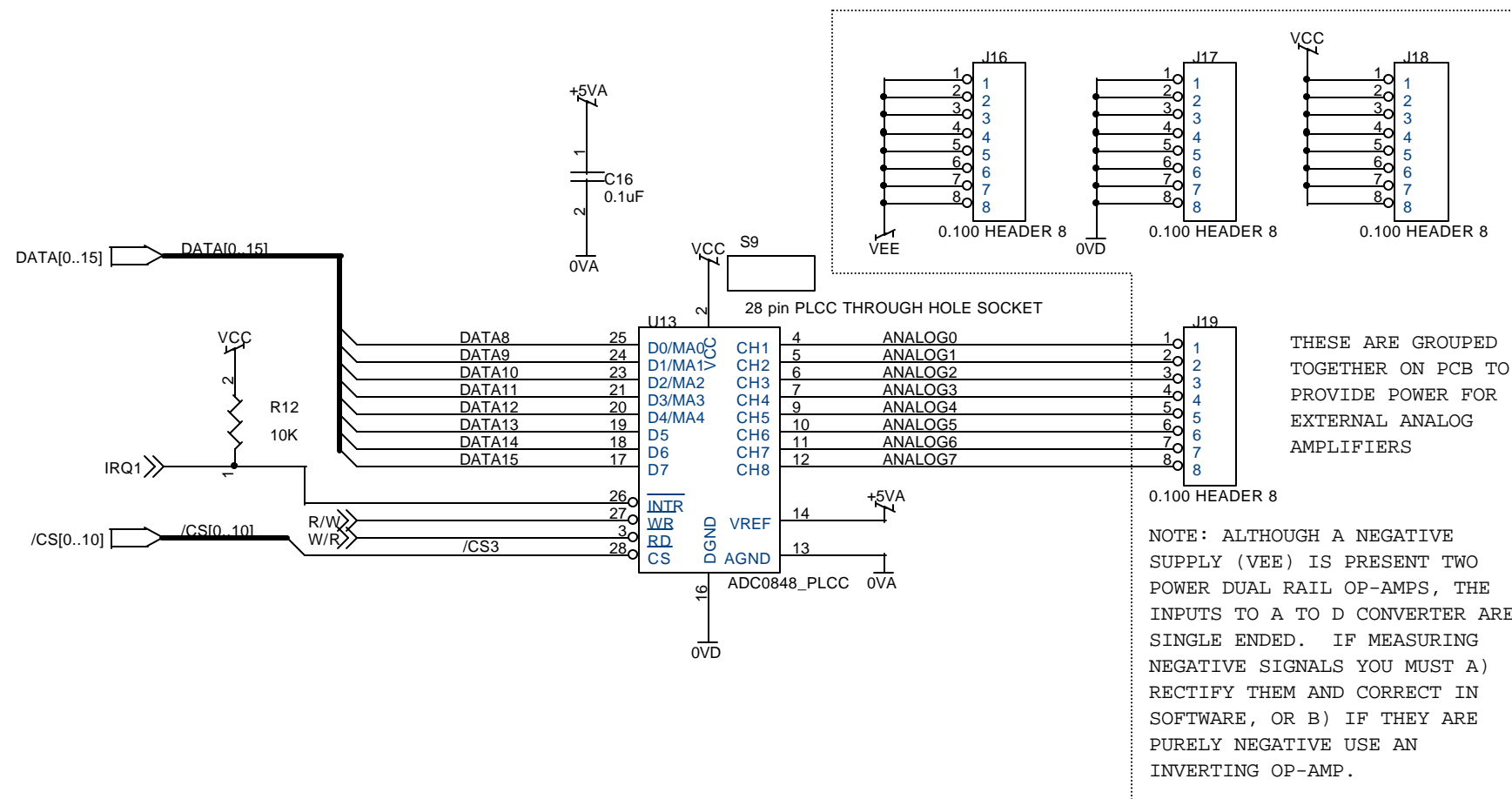
CONNECT JUMPER TO SUPPLY MOTORS FROM SYSTEM POWER, REMOVE IT IF A SEPERATE MOTOR POWER SUPPLY IS USED. THIS JUMPER MUST BE REMOVED IF AN EXTERNAL BATTERY/POWER SUPPLY WILL BE USED TO PROVIDE POWER TO V_MOTOR.



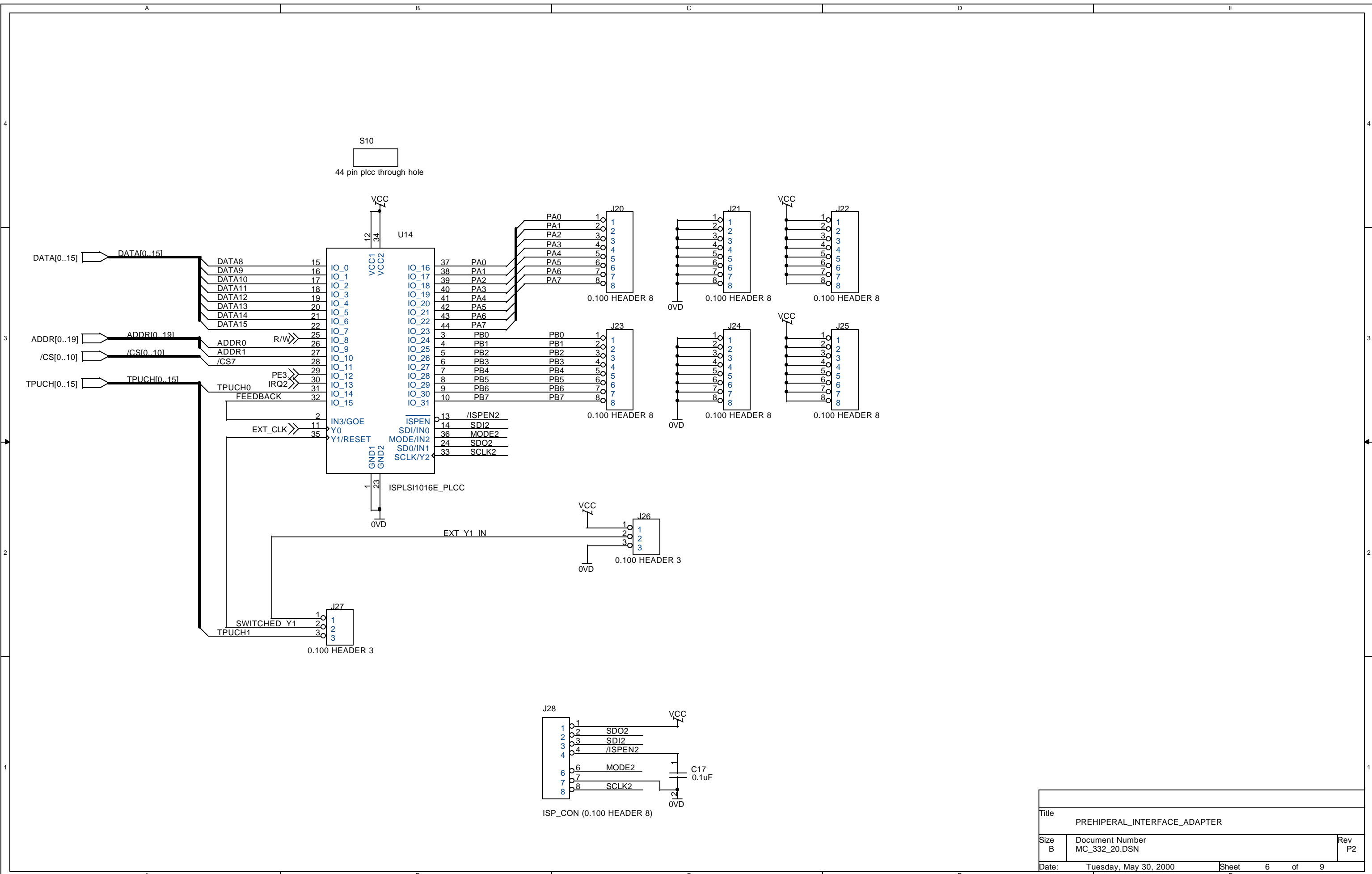
RECOMENDED SUBSTITUTION IS THE POWERTRENDS PT7805

INITIAL TESTING WITH PROTOTYPE BOARD, CURRENT DRAWS OF ONLY 90mA @ 16V WERE REALIZED ALLOWING THE SYSTEM TO RUN WITHOUT HEATSINK ON LINEAR REGULATOR.

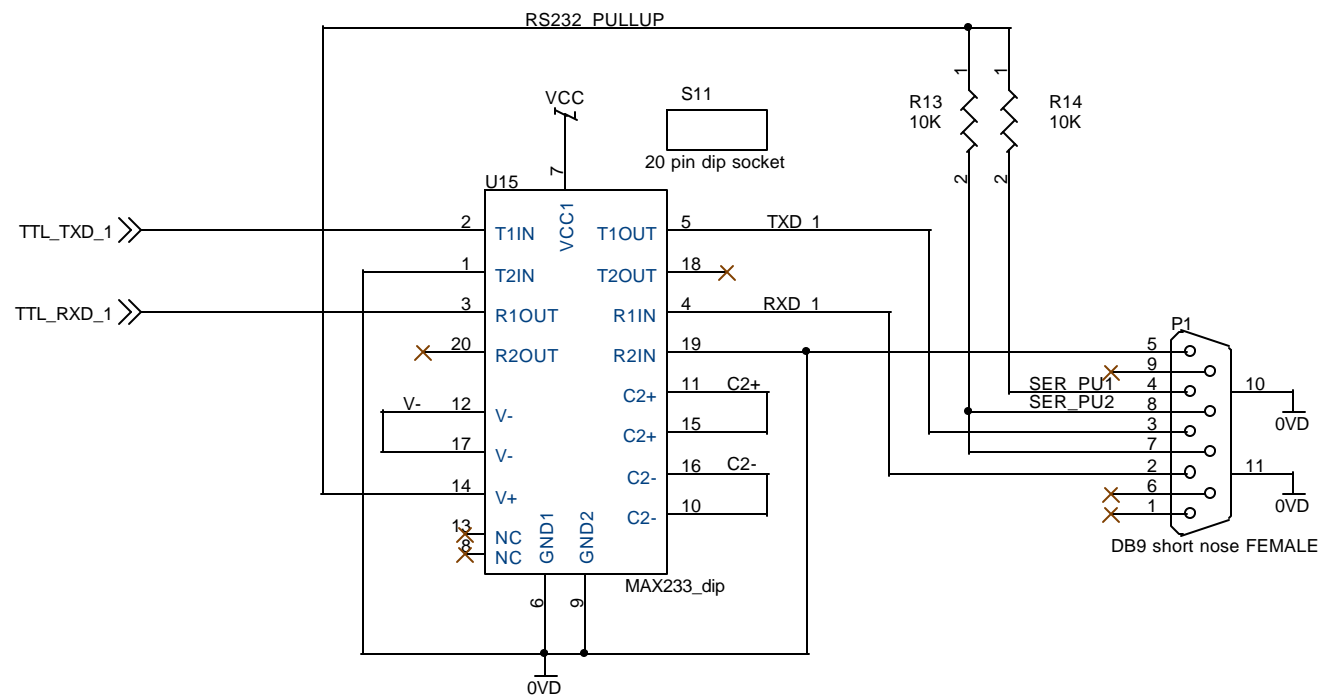
Title		
POWER_SUPPLY		
Size	Document Number	Rev
B	MC_332_20.DSN	P2
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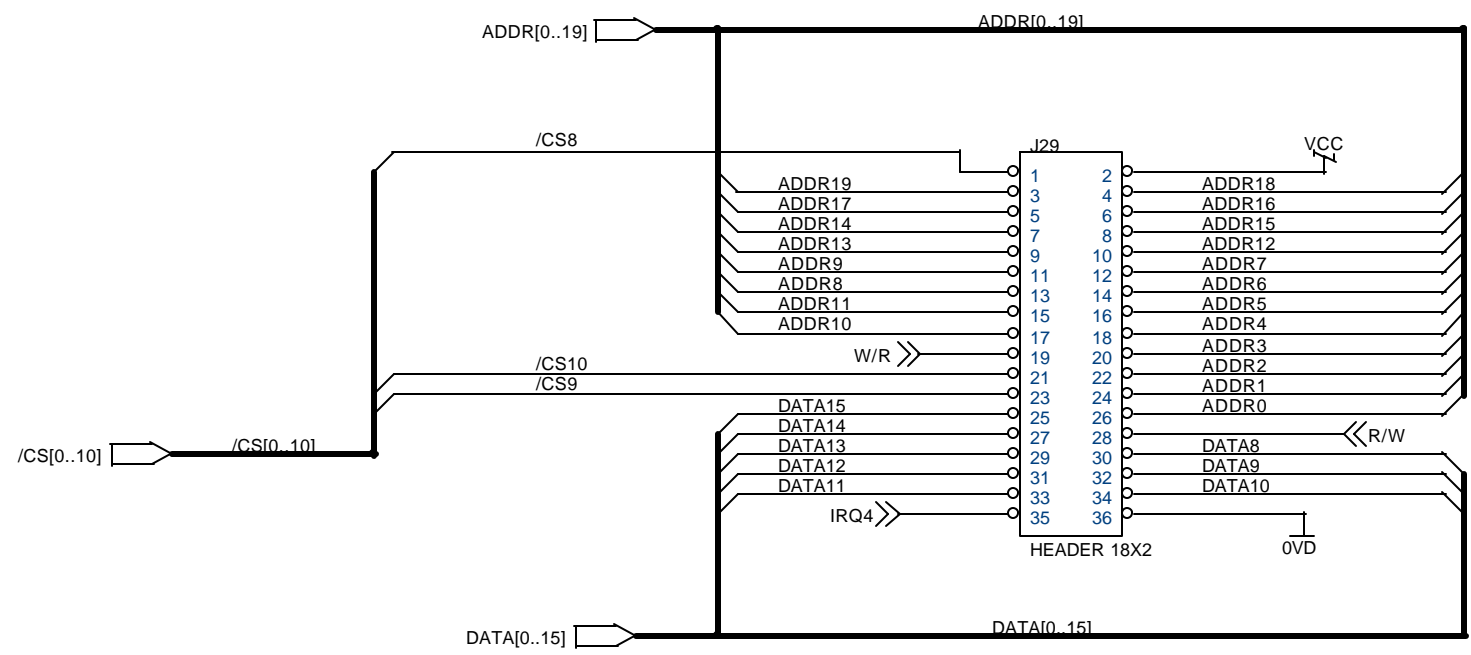
Title		
ANALOG_2_DIGITAL		
Size	Document Number	Rev
B	MC_332_20.DSN	P2
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Title		
PREHIPERAL_INTERFACE_ADAPTER		
Size	Document Number	Rev
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Title		
232_INTF		
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ALSO RECOMENDED FOR USE WITH THIS BOARD ARE .100" NON-POLARIZED CONNECTOR HOUSINGS AND CRIP PINS IN 2,3 & 4 PIN ARRANGEMENTS AND SHORTING BLOCKS

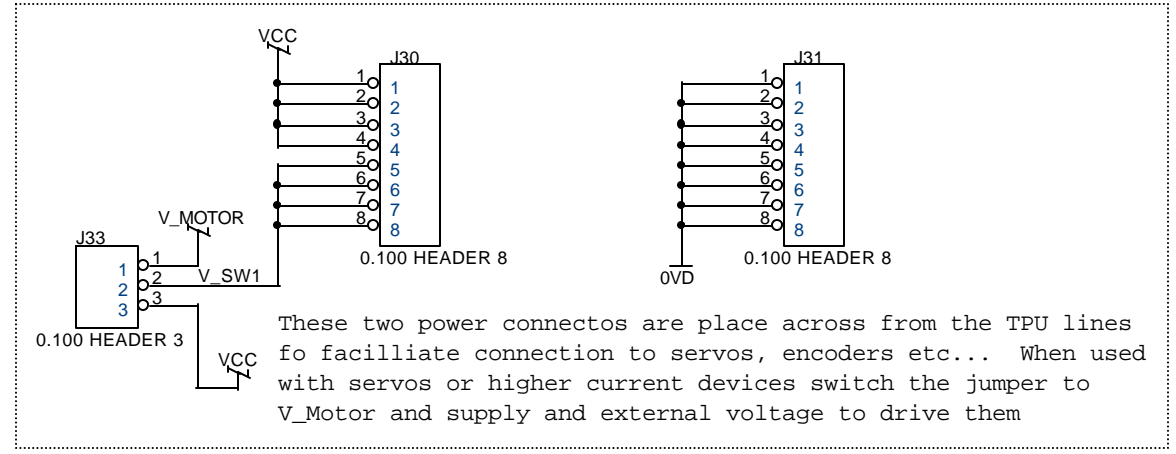
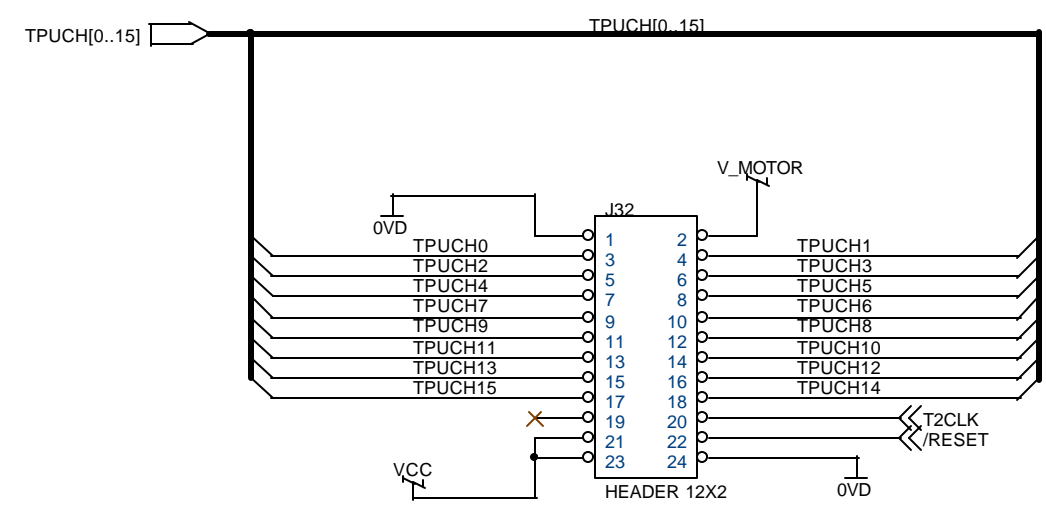
C18
2 PIN CONNECTORS

C19
3 PIN CONNECTORS

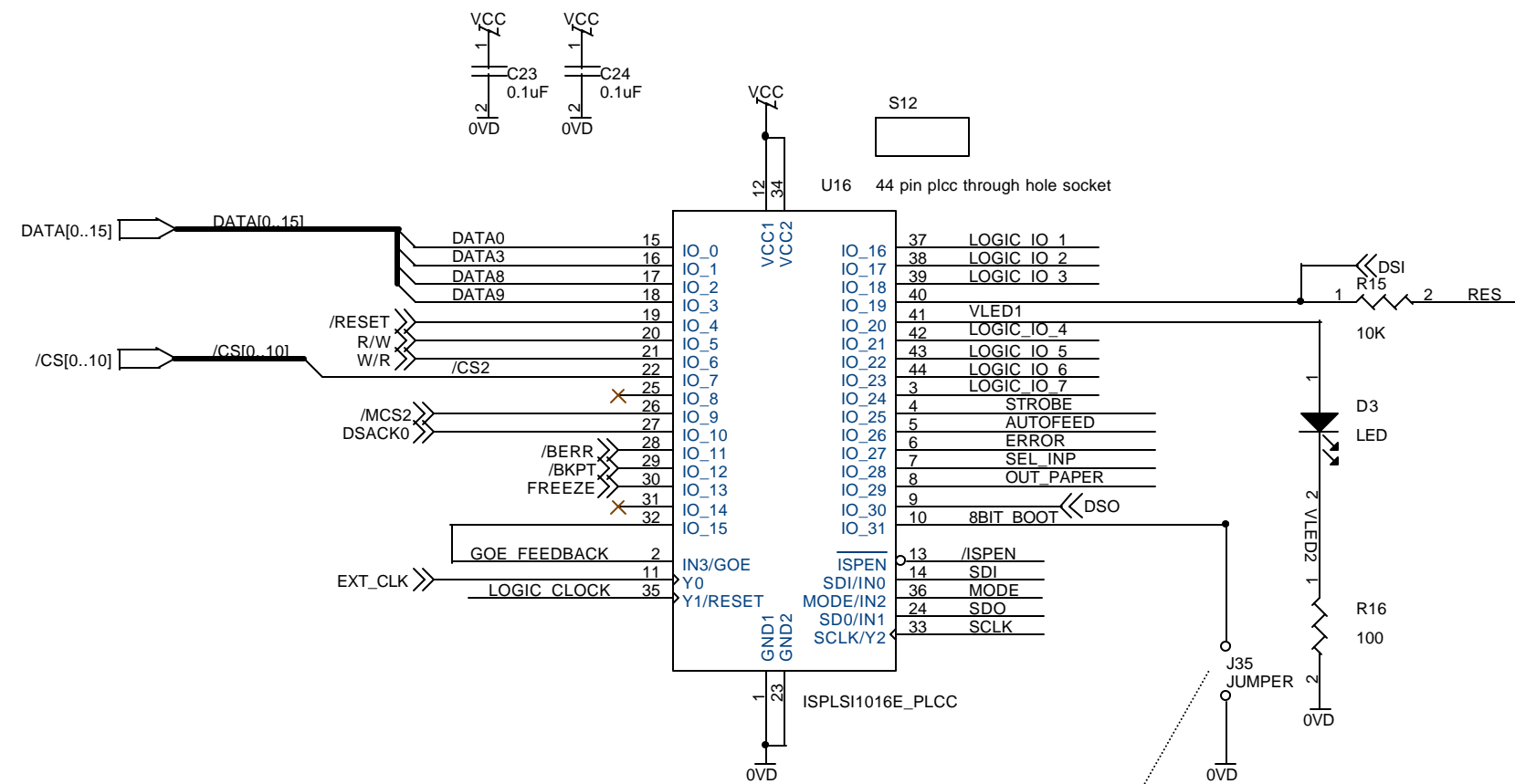
C20
4 PIN CONNECTORS

C21
FEMALE CONNECTOR PINS (22AWG)

C22
SHORTING BLOCKS

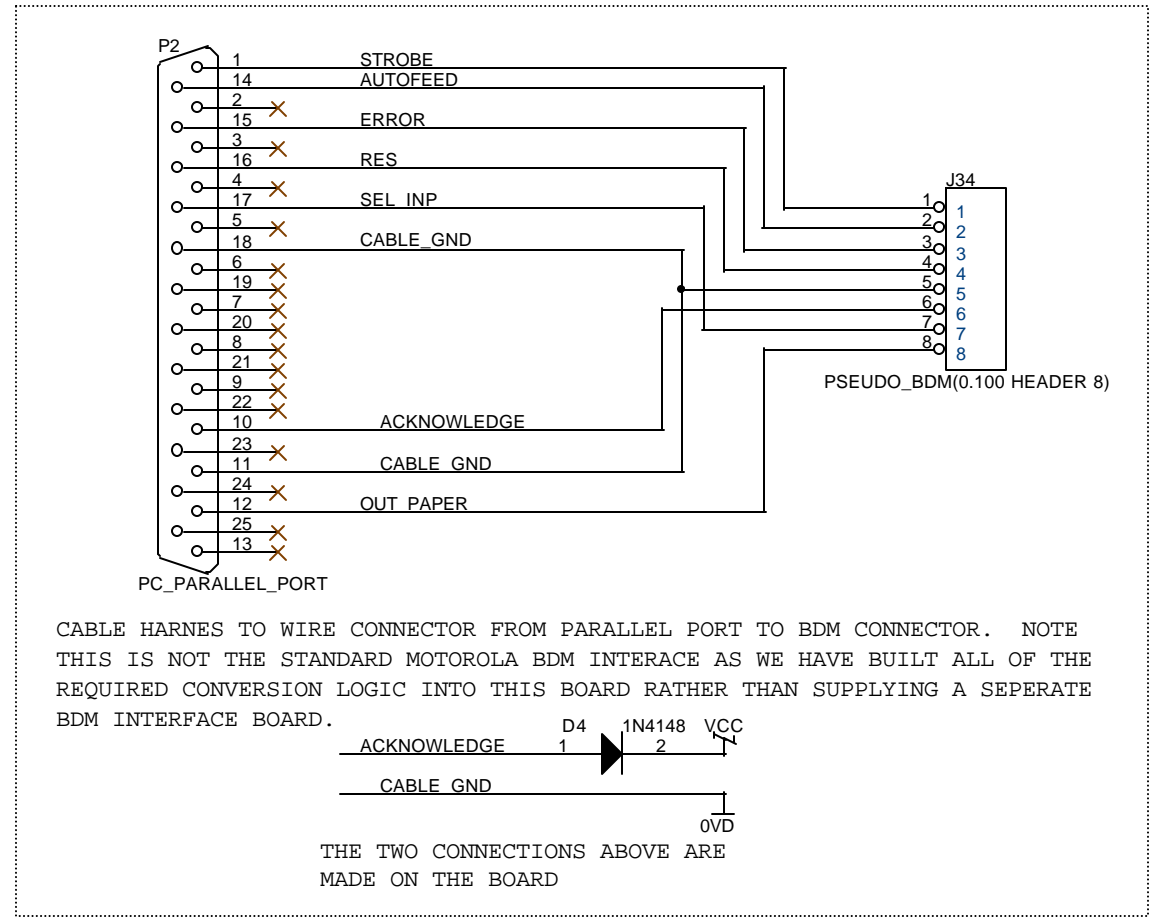
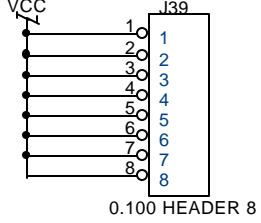
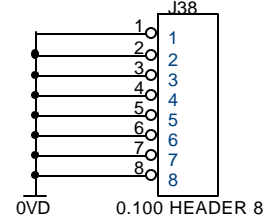
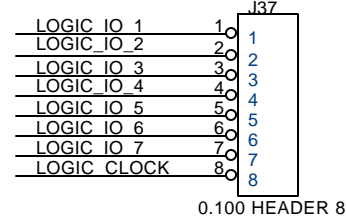
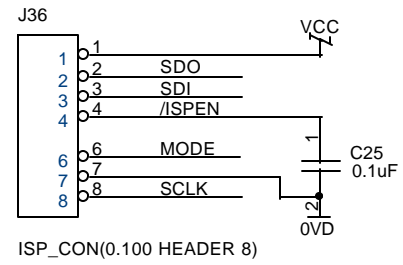


Title		
VERTICAL_STACKING_INTF_BUSS		
Size	Document Number	Rev
B	MC_332_20.DSN	P2
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IF INSTALLED, THE 8 BIT BOOT JUMPER ALLOWS THE SYSTEM TO BOOT FROM A SINGLE 8 BIT RAM, THE EPROM, OR THE FLASH. IF REMOVED /CSBOOT IS 16 BITS WIDE TO BOOT FROM TWO 8 BIT RAMS.

IN SYSTEM PROGRAMMING
HEADER REMOVE PIN #5
FOR KEYED PLUG NO PAD ON
PCB FOR 8 PIN HEADER



Title		
BDM_&_ISP		
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